Docket No.: SON-3173
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Masaaki Bairo

Application No.: 10/584,994 Confirmation No.: 5930

Filed: June 29, 2006 Art Unit: 2826

For: BIPOLAR TRANSISTOR, SEMICONDUCTOR APPARATUS HAVING THE BIPOLAR TRANSISTOR, AND METHODS FOR MANUFACTURING THEM

Examiner: W. W. Kuo

REPLY BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Madam:

This is a Reply Brief under 37 C.F.R. §41.41 in response to the Examiner's Answer mailed on November 11, 2008.

All arguments presented within the Appeal Brief of September 9, 2008 are incorporated herein by reference. Additional arguments are provided hereinbelow.

Claims 9-15 are currently pending in this application. No claims have been allowed.

Among others, the following positions were presented in the Examiner's Answer, each of which will be addressed in turn in this Reply Brief:

ARGUMENT

Claims 9-13

The Final Office Action *readily admits* that U.S. Patent No. 6,307,227 (Fujii) ***fails*** to teach the holes being *simultaneously formed* (Final Office Action at page 4).

The Examiner's Answer *fails* to show holes being *simultaneously formed* within Fujii.

Thus, Fujii *fails* to disclose, teach, or suggest forming base and emitter electrode lead openings within said insulating film, *said base electrode lead opening being formed simultaneous with said emitter electrode lead opening* (Appeal Brief at page 6).

Instead, the Examiner's Answer contends that U.S. Patent No. 5,013,677 (Hozumi) teaches the *missing limitation* that the base electrode lead opening 9b is formed simultaneous with the emitter lead opening 9b (Hozumi at column 6, lines 57-61) for the benefit of realizing the simultaneous production of a transistor and other elements with a simplified process of manufacture (Hozumi at column 7, lines 67-68 - column 8, lines 1-10) (Examiner's Answer at page 7).

In response, the Examiner's Answer fails to show why the skilled artisan would have been motivated to modify the method of Fujii using the process of Hozumi.

In particular, claim 9 of the present application provide for ***FORMING AN INSULATING FILM (2) ON SAID BASE LAYER (18)***, along with ***forming base and emitter electrode lead openings (4, 5) WITHIN SAID INSULATING FILM (2),*** said base electrode lead opening (5) being formed simultaneous with said emitter electrode lead opening (4) (Specification at Figure 3).

However, the process of Hozumi *fails* to show that silicon dioxide film 9 is ***formed on a base layer*** (Hozumi at Figure 1A).

As a consequence, the process of Hozumi is incompatible with the method of Fujii.

U.S. Patent No. 6,885,081 (Morimoto) fails to disclose, teach, or suggest the presence of a bipolar transistor. Instead, the figures of Morimoto depict a capacitor.

- ***Thus, Fujii, Hozumi and Morimoto, either individually or as a whole, fail to disclose, teach, or suggest forming base and emitter electrode lead openings within said insulating film, said base electrode lead opening being formed simultaneous with said emitter electrode lead opening.***

The Office Action *readily admits* that Fujii ***fails*** to teach the step of polishing said conducting film to separate said base electrode lead portion from said emitter electrode lead portion (Final Office Action at page 4).

The Examiner's Answer *fails* to show a step of polishing within Fujii.

The Office Action *readily admits* that Hozumi ***fails*** to teach the step of polishing said conducting film to separate said base electrode lead portion from said emitter electrode lead portion (Final Office Action at page 4).

The Examiner's Answer also *fails* to show a step of polishing within Hozumi.

As a gap-filler, the Examiner's Answer contends it is noted that U.S. Patent No. 6,885,081 (Morimoto) teaches a step of polishing a conducting film to separate electrode lead portions for the benefit of forming individual plugs in via holes (Morimoto at column 6, lines 17-25) (Examiner's Answer at page 7).

In response, no teaching of step of polishing a conducting film to separate electrode lead portions can be found within Morimoto.

Instead, Morimoto arguably discloses that then, *surface polishing by the CMP method* is performed starting with the surface of the tungsten film 14 to *remove the tungsten and titanium*

nitride films other than the film portions filled in the via holes, whereby a plug 14 (same reference number as that for the tungsten film is used for the sake of convenience) made of the titanium nitride film and the tungsten film 14 is formed in each via hole 13, as shown in FIG. 2C (Morimoto at column 6, lines 18-24).

However, Morimoto is ***silent*** regarding portions of the tungsten film 14 being connected prior to surface polishing by the CMP method.

Morimoto is also ***silent*** regarding the separation of one portion of the tungsten film 14 from another portion of the tungsten film 14.

Nevertheless, the Examiner's Answer asserts, *without any supporting evidence*, that since the titanium nitride and tungsten are deposited on and in the via holes 13 (providing a state where the via holes are initially connected through surface layer 14) and then subsequently CMP polished to leave only plugs 14 in the via holes, Morimoto teaches surface polishing by CMP to separate one portion 14 from another portion 14 (Examiner's Answer at page 8).

In response, the theory set forth within the Examiner's Answer is pure conjecture that is unsupported by any teaching within Morimoto.

Note that the Examiner's Answer could also have concocted some other alternative theory of a process that may include partially filling the via holes 13 with titanium nitride and tungsten and thereafter performing a surface polishing by the CMP method to *reduce the height of the second insulating film 12* to the level of the tungsten film 14.

But in the absence of any express or implied teaching within Morimoto, the theory set forth within the Examiner's Answer or any other theory is conclusory at best.

Even still, Morimoto ***fails*** to teach the presence of a bipolar transistor. Instead, the figures of Morimoto depict a capacitor.

Additionally, Morimoto provides that a plug 14 (same reference number as that for the tungsten film is used for the sake of convenience) made of the titanium nitride film and the tungsten film 14 is formed in each via hole 13 (Morimoto at column 6, lines 21-24).

However, Fujii ***fails*** to disclose, teach, or suggest either layer 13 or 15 as being made of a *titanium nitride* film and a *tungsten* film 14. Instead, Fujii discloses the presence of a base *polysilicon* 13 (Fujii at column 7, lines 33-34) and an emitter *polysilicon* 15 (Fujii at column 8, line 1).

In this regard, the Examiner's Answer ***fails*** to provide any objective evidence that the either layer 13 or 15 of Fujii could be subjected to the surface polishing of Morimoto.

However, Hozumi ***fails*** to disclose, teach, or suggest layer 11 as being made of a *titanium nitride* film and a *tungsten* film 14. Instead, Hozumi discloses the presence of a *polycrystal silicon* layer 11 (Hozumi at column 3, line 62).

In this regard, the Examiner's Answer ***fails*** to provide any objective evidence that the polycrystal silicon layer 11 of Hozumi could be subjected to the surface polishing of Morimoto.

Yet, the Examiner's Answer fails to explain why the skilled artisan would have been motivated to replace either polysilcon layer 13 or 15 of Fujii, or polycrystal silicon layer 11 of Hozumi, with tungsten film 14 of Morimoto.

- ***Thus, Fujii, Hozumi, and Morimoto, either individually or as a whole, fail to disclose, teach or suggest the step of polishing said conducting film to separate said base electrode lead portion from said emitter electrode lead portion.***

Claim 14

Claim 14 is drawn to a method for manufacturing a bipolar transistor that includes the step of depositing a silicide (7) onto a polished surface of said conducting film (40, 50).

The Examiner's Answer *readily admits* that Fujii, Hozumi, and Morimoto ***fail*** to disclose, teach or suggest a step of depositing a silicided onto a polished surface of said conducting film (Examiner's Answer at page 9).

Nevertheless, the Examiner's Answer asserts that U.S. Patent Application Publication No. 2003/0235984 (Besser) teaches that it is advantageous to use silicided instead of aluminum in order to provide contacts that are reliable, thermally stable, and have lower resistivity (Besser at paragraph [0003]) (Examiner's Answer at page 9).

In response, Besser arguably teaches that during silicidation, silicon from active regions 120 and gate region 130 diffuses into metal layer 150 and/or metal from metal layer 150 diffuses into silicon-containing active regions 120 and gate region 130 (Besser at paragraph [0025]).

However, Besser ***fails*** to disclose, teach, or suggest gate region 130 as being polished.

- ***Thus, Fujii, Hozumi, Morimoto and Besser, either individually or as a whole, fail to disclose, teach or suggest depositing a silicide onto a polished surface of said conducting film.***

Claim 15

Claim 15 is drawn to the method for manufacturing a bipolar transistor as described in claim 14, further comprising the step of depositing an interlayer insulator (30) onto said silicide (7) and said insulating film (2).

The Examiner's Answer seems to attempt a substitution of a first wiring layer 18 of Fujii with a silicide of Besser (Examiner's Answer at page 9).

In response, a review of Fujii reveals a first layer contact 17 connected to *gate polysilicon 8* (Fujii at Figure 9).

Likewise, Besser arguably teaches that during silicidation, silicon from active regions 120 and gate region 130 diffuses into metal layer 150 and/or metal from metal layer 150 diffuses into silicon-containing active regions 120 and *gate region 130* (Besser at paragraph [0025]).

However, Fujii in view of Besser fails to show why the skilled artisan would have been motivated to modify Fujii by replacing a first wiring layer 18 of Fujii with a silicide of Besser when Besser *fails* to teach the presence of a wiring layer, and when Besser fails to disclose, teach, or suggest a silicided contact similar to first layer contact 17 of Fujii.

CONCLUSION

There is no concession as to the veracity of Official Notice, if taken in any Office Action.

An affidavit or document should be provided in support of any Official Notice taken. 37 CFR 1.104(d)(2), MPEP § 2144.03. See also, *Ex parte Natale*, 11 USPQ2d 1222, 1227-1228 (Bd. Pat. App. & Int. 1989)(failure to provide any objective evidence to support the challenged use of Official Notice constitutes clear and reversible error).

For the foregoing reasons, all the claims now pending in the present application are allowable, and the present application is in condition for allowance.

The prior art of record fails to disclose, teach or suggest all the features of the claimed invention.

For at least the reasons set forth hereinabove, the rejection of the claimed invention should not be sustained.

Therefore, a reversal of the rejection of February 22, 2008 is respectfully requested.

If any additional fee is required or any overpayment made, the Commissioner is hereby authorized to charge the fee or credit the overpayment to Deposit Account # 18-0013.

Dated: December 5, 2008

Respectfully submitted,

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